

Neuromodulator Device Scrap Reduction Using DMAIC Methodology

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Abstract — *This research project was focused in the Scrap reduction in a final electrical test area of a medical device company. The scrap is defined as the number of dollars per units resulting from the cost of rejected units coming out of a process divided by the number of units which are released successfully. Only good units (no retest & rework allowed) are counted as coming out of an individual process.*

In order to reduce the Scrap, the DMAIC methodology was used [1]. DMAIC is an acronym for a series of steps used to measure defects in business processes and improve profitability. The term DMAIC stands for the five main steps in the process: Define, Measure, Analyze, Improve and Control.

This research seeks to reduce the Scrap on this manufacturing area where the neuromodulator device is finally verified electrically. This is important for the process because it will reduce unnecessary Scrap related to this false failure. DMAIC methodology brings a structure and the tool to identify and solve the problem. In this case, reduce the Scrap in a medical device company.

Key Terms – *Cost-Saving, DMAIC, Quality, Scrap.*

PROBLEM STATEMENT [2]

The cell dedicated to testing and verified of the neuromodulator has had an increase in FRAM failures at Post Sterile test area. This electrical failure is the top offender at this cell since the beginning of this product line in February 2018. With the reduction of this defect, a significant Scrap reduction can be achieved [2]. The goal is to reduce and maintain Post Sterile false failures per FRAM test code. In order of achieve this goal the purpose is to use the DMAIC project methodology.

RESEARCH DESCRIPTION

This research is about reducing the Scrap at the manufacturing area where the neuromodulator is finally tested. This is important to the process to reduce Scrap and the negative impact on product released.

RESEARCH OBJECTIVES

This project aims to achieve a reduce Scrap at maintain the Post Sterile manufacturing area by 15%. This will reduce the Post Sterile false failures, cycle time, scrap and maintain a properly flow rate.

RESEARCH CONTRIBUTIONS

This project seeks to achieve a reduction in Scrap. This improves the process to move faster to the next operation with a positive impact in the Scrap metric. The process flow will be continuous and linear. With less failures, the cost associated to Scrap can be reduced significantly, since at this level the device associated cost is \$1,512.98. This reduction will represent approximately \$150,000 yearly for this Arecibo medical device company.

LITERATURE REVIEW

An implantable pulse generator neuromodulator (SCS – Spinal Cord Stimulation) delivers mild electrical stimulation to nerves along the spinal column, modifying nerve activity to minimize the sensation of pain reaching the brain. The neuromodulator is designed for patients who have an abnormal back, pelvic or abdominal pain. Implanting a neuromodulator is considered a minimally invasive ambulatory surgical technique. Usually, a patient will try a temporary externalized SCS (Spinal Cord Stimulation) system, and if pain is

reduced by at least 50%, the patient returns to receive an implanted system. The neuromodulator history began in the 1960s. The U.S. Food and Drug Administration (FDA) first approved SCS in 1989 to relieve chronic pain from nerve damage in the trunk, arms or legs. The neuromodulator evolved and now is an implantable medical device with batteries capable of lasting up to seven years and the body of the device is about 4-5 centimeters long.

Current device consists of a titanium body and silicon head (Figure 1). Internally, the titanium case encloses the chip (hybrid PCB) containing the program and contains the battery. The header is a silicon casting which encloses the electrode connectors.



Figure 1
Device

General Concepts of DMAIC Methodology

DMAIC is an acronym for a series of steps used to measure defects in business processes and improve profitability. It is one of two key methods used to implement Six Sigma, a quality improvement program introduced in 1986 by Motorola, a U.S. technology and communications company. By identifying defects, a company can eliminate errors and accurately determine quality. Then, the company can use those findings to figure out a solution to a detected problem. Today, Six Sigma methods are used across a broad range of industries to improve both processes and profitability.

The DMAIC problem solving method is a roadmap that can be used for any projects or quality improvements that needs to be made. The term

DMAIC stands for the five main steps in the process: Define, Measure, Analyze, Improve, and Control.

Define: Define the problem, the process, and the project goals. In Six Sigma, it is imperative that the problem is specifically defined. Saying that business is slowing down is a poorly defined problem. Instead, the problem should be clearly established in quantitative terms. So, a good Six Sigma problem definition would say that business has had a 35% decrease in net sales in the past two consecutive quarters.

Measure: Measure and collect data that will determine the factors that have influence over the outcome of the process or procedure.

- **Analyze:** The data is analyzed using statistical tools to assess whether the problem is real (and solvable) or random, which makes it unsolvable within the Six Sigma framework.
- **Improve:** If the problem is real, the Six Sigma team identifies solutions to improve the process, based on the data analysis.
- **Control:** Control planning, including data collection and control mechanisms, is required to ensure that the solutions are sustainable and deliver peak performance. It also ensures that early deviations from the target do not materialize into process defects.

PROJECT METHODOLOGY [3]

In order to achieve the goal of reduce Scrap at Post Sterile test area related to FRAM failures, the DMAIC tools project methodology was used.

At the Define steps, the following tools will be used:

- **Project Charter:** is a statement of the scope, objectives and participants in a project. It provides a preliminary delineation of roles and responsibilities, outlines the project objectives, identifies the main stakeholders, and defines the authority of the project manager. It serves as a reference of authority for the future of the project.

**Table 1
Project Charter**

Problem Statement:	An increase in FRAM failures at Post Sterile test area affected significantly scrap goal and negatively impacting the UPL.
Goal:	Reduce FRAM failures with a final Scrap reduction of 15% by 31 Dec 2019.
Metric definition:	Scrap Reduction

- Voice of the Customer (VOC): is a market research technique that produces a detailed set of customer wants and needs, organized into a hierarchical structure, and then prioritized in terms of relative importance and satisfaction with current alternatives.

At the Measure steps, the following tools will be used:

- Control Charts: also known as P-Charts or process-behavior charts. In statistical process control, are tools used to determine if a manufacturing or business process is in a state of statistical control.
- Other tools could be used during the measure step.

For the following steps (Analysis, Improvement, and Control) tools to be used were determined during the project process according the previous steps results.

RESULTS AND DISCUSSION [2]

The results obtained through the five phases of the DMAIC methodology are:

Define - As part of this Define phase, the VOC tool was performed to determine what the customer wants and needs. The results were illustrated in Table 1.

**Table 2
Voice of Customer (VOC)**

Key Customer	Operation Manager Supervisor
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Approach	<p>Research possible root causes per PFMECA.</p> <p>Observed similar failures with approved reworks on Post Sterilization areas on other devices product lines.</p> <p>Speak to process owners and developers' experts to obtain their recommendation on areas to focus.</p> <p>Based on the PFMECA, other similar failures on different devices areas, their recommendations devices were analyzed and documented.</p> <p>Revise the defects data daily.</p> <p>Involve operators, technicians, and supervisors.</p> <p>Share data with the team.</p> <p>Gather feedback for evaluation.</p> <p>Evaluate if improvements have impact on metrics.</p>
Customer Concerns	<p>Finances</p> <p>False Failure Scrap</p> <p>Daily Output</p>
Boundaries (in scope vs out of scope):	<p>Project will be focused in Scrap reduction.</p>

From the VOC was noted that the greatest concern was to confirm that a high percentage of FRAM failures were false failures.

To confirm a high percentage of false failures, the following assessment were performed to 32 units sample:

FRAM means:

- **Ferroelectric Random Access Memory**
 - Is a non-volatile memory that can hold data even after it is powered off. This memory is not affected by magnetic fields as there is no ferrous material (iron) in the chip and offer the same functionality as a flash memory.
- **Objective Evidence Recap from Q1 2019**
 - 1st Top Off – FRAM ERR Check Failure Mode
 - FRAM Scrap = \$54,467.28
 - FPY at Post Sterile Level 98.9% from an expected 99.5%
 - FRAM represents 13.8% of total Scrap
 - FRAM RR% = 0.69%

For Analysis:

- 32 devices that failed due to FRAM ERROR were verified.
- Image were performed using Image Analyzer tool.
- Image provide exact date and time when the error occurred.
- After firmware was downloaded the error appears.
- Firmware was downloaded at Post Header electrical test level.
- Suspected operations that were analyzed as part of PR analysis in order to find a high failure rate trend are:
- Immediately after Post Header Test
- Sterile Tray Seal
- Sterilization Process

ATE PR Analysis – 32 Samples Experiment

Results:

- Immediately After Post Header – 6 units – 19.35%
- Before tray seal – 8 units – 25.81%
- Under tray seal process – 0%
- After tray seal – 17 units – 54.84%
- Before sterilization – 0%
- Under sterilization process – 0%
- After sterilization – 0%

Next Steps:

- Close analysis between Post Header test and Sterile tray seal process.
- Immediately After Post Header stay under analysis
- Before tray seal stay under analysis
- Under tray seal stay under analysis
- After tray seal stay under analysis (highest rate)
- Before sterilization removed from the analysis
- Under sterilization process removed from the analysis
- After sterilization removed from the analysis
- In conclusion any test area induced the error per temperature or other variable.

The areas to be focus will not be the previous provided areas. Device memory errors or software soft errors will be verified.

Measure - Every part rejected is documented at the disposition area of the traveler and then entered into the database. All data was validated by the project leader, to assure accuracy of the data entry process.

Figure 2 shows the first pass yield reported for the Post Sterile Test Area since 2018.

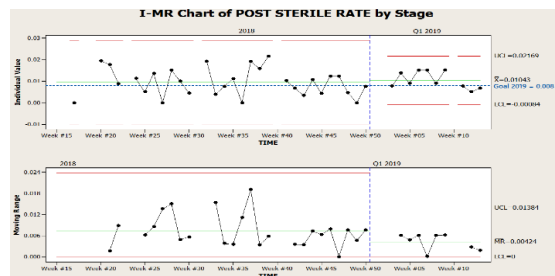


Figure 2

I-MR Chart of Post Sterile Rate by Stage

It is observed that the FPY (First Pass Yield) increase for the Post Sterile Test Area on 2019, however the top offender with the highest cost still present.

Figure 3 shows the Scrap costs reported due to FRAM failures on 2018 and 2019.

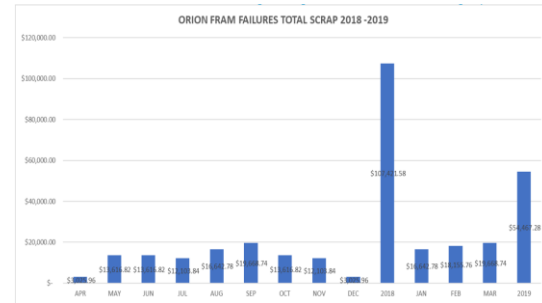


Figure 3

Orion Fram Failures Total Scraps Costs 2018-2019

From the Figure 4 (which represents the rejection rate Pareto graph) was observed that RR average per this failure is less than 1.0%. So, FPY was not an issue; the cost of the unit at this level can't allow false failures at this level.

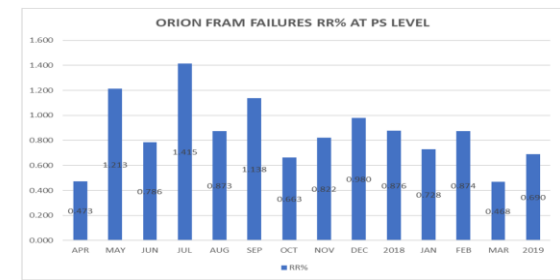


Figure 1
Pareto Diagram

Analysis - the Analysis of the data collected shows that FRAM failure are the major offender that impact Scrap goal in the data set. The following steps were performed to determine if the units can reload the firmware and the pass Post Sterile Test successfully and continuously.

ATE PR Analysis – 32 Samples Experiment

Next Steps

- 32 scrapped units were segregated for evaluation
- DWLD TCC was performed to each unit
- 2 units were unable to DWLD TCC (Err - 8003)
- Post Header Test was performed on November 2018 to each unit
- 29 units pass firmware reload successfully
- 1 failed Load Product FW
- Post Sterile Test was performed on November 2018 to each unit
- 28 units pass successfully
- 1 unit failed per FRAM Err

Next Steps:

- Device Image was performed on December 2018 to each unit
- 28 units pass successfully
- Device Image was performed on January 2019 to each unit
- 28 units pass successfully

ATE PR Analysis – 32 Samples Experiment

Final Summary

- In summary the obtained results are:
- 87.5 % confirmed good devices (False Failure)
- 6.3 % failed unable to DWLD TCC not open Physical Channel
- 3.1 % failed Post Header Test unable to Load Product FW
- 3.1 % failed Post Sterile Test after firmware was re-downloaded (FRAM Err)

Final Summary

- A total of 71 devices failed per this condition during 2018
- A total of \$107,421.58 was launched in Arecibo during 2018 per FRAM failure mode
- Rejection Rate of .876 % was obtained during 2018 per this condition (71 Device Failed/8102 Manufacturing Units)
- Experiment can't confirmed a process induced error
- In addition:
- A total of 200 devices failed per this condition during 2018 at Plano, Texas
- A total of \$302,396.00 was launched in Plano during 2018 per FRAM failure mode.

ATE PR Analysis – 32 Samples Experiment

What we need to do?

- Concentrate efforts on the 87.5% of false failures.
- Dedicate a team to confirm a soft error on test software and corrected.
- Validate a test retest for this particular failures if necessary.

What can we get?

- 87.5% of savings on this particular failure mode
- In comparison with 2018
 - > \$93,993.88 (Arecibo, PR)
 - > \$264,771.2 (Plano, TX)
- In comparison with Q1 2019
 - > \$47,658.87

\$235,646.63

in savings for Arecibo for the last 1.5 years

Figure 5 shows the expected Scrap costs improvement due to FRAM failures without 87.5% of confirmed false failures.

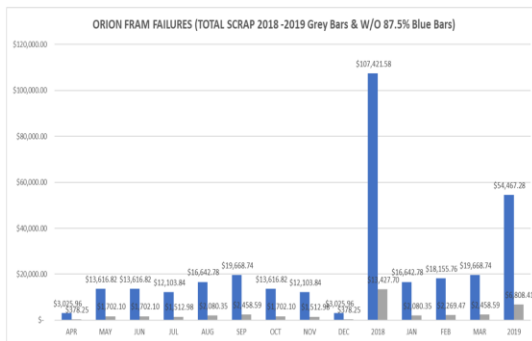


Figure 5
Expected Scrap Costs Improvement

Since the major offenders are the 87.5% of confirmed false failures per FRAM test code, the project target will be focused in reducing the false failures. The process should still be able to capture real failures related to this code.

Improvement - From the results obtained in the analysis phase, it was determined to update the Post Header test software, which is the one that load the firmware per device model previous the device was tested at Post Sterile Test area. Most of the FRAM errors detected at Orion Post-Sterile test system are one SED (Single Error Detection) or DED (Double Error Detection) FRAM error. The FRAM error appears to occur within 24 hours after initial installation of production firmware at Post-Header.

Analysis of test data for all the failed devices didn't show any correlation to the JUNO IC manufacturer lot, manufacturing location or manufacturing period. Analysis of test data for all the failed devices shows that the devices have correct voltage levels during the Orion IPG manufacturing process. Analysis of test data for all the failed devices shows that Orion IPG production firmware versions 1.0, 1.1 and 1.2 had similar FRAM error failure rates. Over 94% of the Orion IPG FRAM errors are fixed within the first 24 hours after Orion Post-Header test and no more FRAM errors were observed after 24 hours. Analysis of test data for all the failed devices shows that the FRAM error occurred before Orion IPG sterilization process. All attempts to reproduce a FRAM error on Orion IPGs that previously failed for FRAM error were not successful.

Analyzing test data and test logs resulted in finding that at least 2 Clear FRAM functions at Orion Post-Header test system resulted in a FRAM error failure rate decreasing from 0.809% to 0.0146%. This Juno IC issue is documented in Unity00095328 SWR that FRAM errors are avoided by writing data twice to FRAM. The 2 Clear FRAM functions in succession at Orion Post-Header test system essentially performed 2 data writes in FRAM.

Based on results from section 12.1 step 29, it was shown that performing at least 2 Clear FRAM functions at Orion Post-Header test system prior to performing product firmware download significantly reduces FRAM error failure rate. In summary, now at this test level, the test station should be able to load firmware, verify memory errors, and correct, if it's necessary, previous sterilization and Post Sterile Test. This second Clear FRAM verification was implemented under software code resulting in satisfactory yield improvement; therefore, a significant Scrap reduction. All steps performed for the validation of this software change were documented under Engineering Test Report **90511139**.

Control - In this phase of the project it was necessary to establish the following controls to perpetuate the improvements in the process. It was

specified a new software change (**90362743 Rev B**), was updated at 5 Post Header Test Stations and documented under an Unscheduled Work Order. In addition, process monitoring in a weekly basis is still in place to monitor Post Sterile Test area behavior.

CONCLUSION [2]

This project validated the use of the DMAIC methodology to reduce Scrap in a Neuromodulation product line of a medical device company. The DMAIC methodology brings a structure for the improvement process. The results obtained are show in the following comparison of the Scrap reduction and FPY behavior (see Figure 6 and 7).

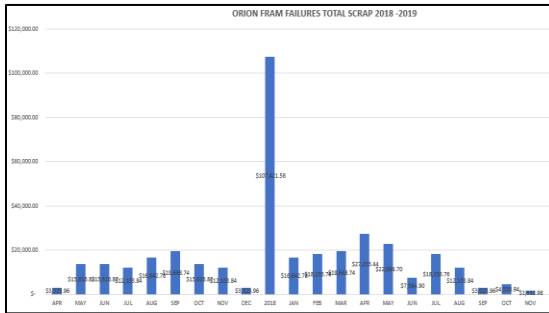


Figure 6

Improvement was Implemented on 02 Sep 2019

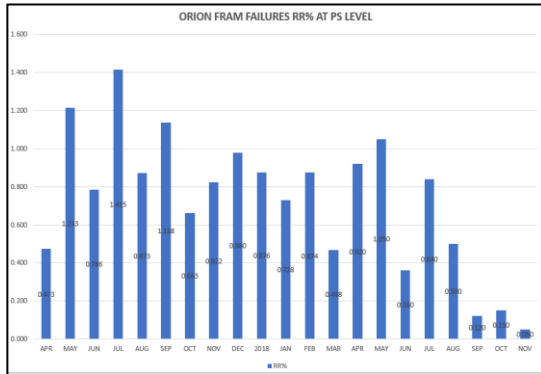


Figure 7

Rejection Rate Favorability after September 2019

These graphs show populations evaluated before and after implementation. Effects are notable. Since the savings for the past three months, in comparison with the beginning of the year, are close to \$40,000 per month; so, there is a significant difference between populations prior and after this project.

Prior Improvement

Jan 2019 – Aug 2019 = \$357,063.08

Average per month = \$44,632.89

After Improvement

Sep 2019 – Nov 2019 = \$9,077.88

Average per month = \$3,025.96

Based on the results, the goal to reduce Scrap by a 15% using the DMAIC methodology was achieved and exceed successfully the expected output.

REFERENCES

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